UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,460	07/30/2003	Darel Emmot	200205912-1	9164

22879 7590 09/28/2007

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

MAIL DATE	DELIVERY MODE
09/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/630,460	EMMOT ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

Claims 1-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The amendments to claims 1, 11, and 20 constitute new matter. If Applicants disagree, Applicants are required to point to the original filed specification by citing page and line numbers for support.

Claims 1-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 20, the language "comprises a plurality of signal of signal lines of the system bus" is unclear. Further, it is unclear what may be included in the "collectively, the conductive pins of the integrated circuit component ... signal lines of the system bus."

Claims 1-10 are directed to an apparatus. However, the essential structural cooperative relationships between elements in the claims such as "logic" (line 2), "logic" (line 4), "logic for controlling," "first portion of system bus," "second portion of system bus," "integrated circuit component," and "second integrated circuit component"

have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2172.01.

Claims 10-19 are directed to an apparatus. However, the essential structural cooperative relationships between elements in the claims such as "first logic", "second logic", "logic for controlling," "portion of system bus," "plurality of companion integrated circuit components" "integrated circuit component," and "remote component" have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2172.01.

Claims 20-24 are directed to an apparatus. However, the essential structural cooperative relationships between elements in the claims such as "first set of conductive pins," "second of conductive pins," "additional conductive pins," "portion of a system bus," "integrated circuit component," and "companion integrated circuit component" have been omitted, such omission amounting to a gap between the necessary structural connections. MPEP 2172.01.

MPEP 2172.01 requires that relationships between elements recited in claims must be specified. Specifically, MPEP requires interrelation and structural relationships between essential elements in the claims. The claimed elements, as defined in the originally filed specification and identified above, are essential elements to the claimed invention. Since they are essential elements as defined by the originally filed specification, their structural cooperative relationships must be provided in the claims. Further, it is also clear that the claimed elements as identified above, function simultaneously, are directly functionally related, directly intercooperate, and/or serve

independent purposes, as evidenced from the originally filed specification. If Applicants do not agree with the Examiner that the claimed elements as defined by the specification and identified above, are not essential elements to the claimed invention, Applicants are required to state on the record that this is the case. Further, if Applicants disagree with the Examiner that the above identified elements, as defined by the originally filed specification, are essential elements to the claimed invention, and that the above identified elements are directly functionally related, directly inter-cooperate, and/or serve independent purposes, it is requested that Applicants provide evidences showing that the identified elements are not essential elements to the claimed invention, do not function simultaneously, are not directly functionally related, do not directly inter-cooperate, and/or do not serve independent purposes; and state on the record that this is the case.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4-13, and 15-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Estakhri et al. (Estakhri, 6,172,906).

At the outset, it is noted that new limitations added to the claims by the amendment filed 2/2/2007 will be fully addressed under "Response to Arguments."

As broadly drafted, these claims do not define any structure that differs from Estakhri.

With regard to claim 1, Estakhri discloses an integrated circuit component (Figs. 1 and 6a, shown below:)

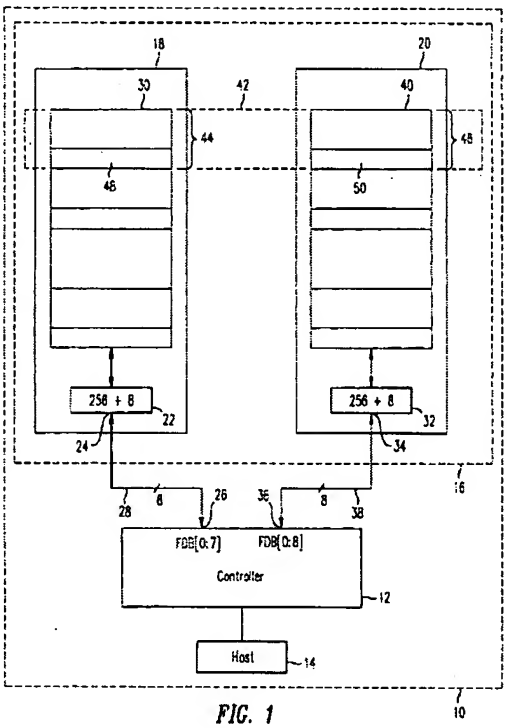
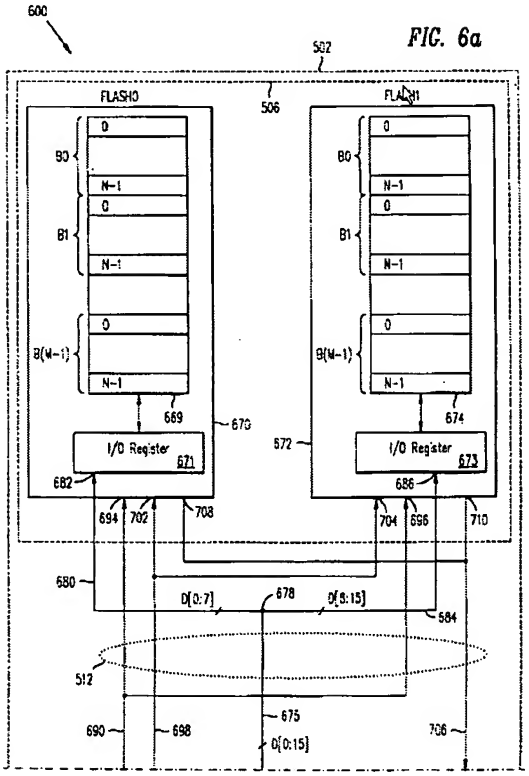


FIG. 1



comprising: logic (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises "logic"; see at least column 2, lines 28-37; column 6, lines 57-65) capable of being configured to interface with a first portion of a system bus (28/680; column 1, line 31 to column 2, line 3; column 7, line 1-9); and logic (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "logic"; see at least column 2, lines 28-37; column 6, lines 57-65) capable of being configured to interface with a companion integrated circuit (18/670 or 20/672; column 1, line 31 to column 2, line 3; column 6, lines 57-65) and to receive information

that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus (38/684; column 1, line 31 to column 3, line 2; column 7, lines 1-9).

With regard to claim 2, Estakhri further discloses a link layer control logic in both the logic capable of being configured to interface with the first portion of the system bus and the logic capable of being configured to interface with the companion integrated circuit (it is clear that the controller (12/510; column 1, line 31 to column 2, line 3; column 6, lines 10-29) linking both logics to provide unified bus logic configured to consolidate information received from both logics interfaced with the first portion of the system bus (28/260; column 1, line 31 to column 2, line 3; column 7, line 1-9) and the companion integrated circuit 18/670 or 20/672), the link layer control logic (12/510; column 1, line 31 to column 2, line 3; column 6, lines 10-29) being configured to exchange link layer control information, such that both the logic capable of being configured to interface with the first portion of the system bus and the logic capable of being configured to interface with the companion integrated circuit (both logics interfaced with the first portion of the system bus (28/680; column 1, line 31 to column 2, line 3; column 7, line 1-9) and the companion integrated circuit 18/670 or 20/672; column 1, line 31 to column 2, line 3; column 6, lines 57-65) possess complete link layer control information for the data being communicated over the system bus (it is clear that the controller (12/510; column 1, line 31 to column 2, line 3; column 6, lines 10-29) provides unified bus logic configured to consolidate information received from both logics interfaced with the first portion of the system bus (28/680; column 1, line 31 to

column 2, line 3; column 7, line 1-9) and the companion integrated circuit 18/670 or 20/672; column 1, line 31 to column 2, line 3; column 6, lines 57-65).

With regard to claim 4, it is clear that the controller (12/510) provides unified bus logic configured to consolidate information received from both logics interfaced with the first portion of the system bus 28/260 and the companion integrated circuit 18/670 or 20/672).

With regard to claim 5, it is clear that the controller (12/510) or the so-called "functional logic" performs at least one logic operation for the integrated circuit component.

With regard to claim 6, it is clear that the system bus comprising two split buses 28/260 and 38/684 is a point-to-point serial communication bus.

With regard to claim 7, it is clear that the memory controller (12/510) or the so-called "functional logic" performs the logic operation of a memory controller.

With regard to claim 8, it is clear that the memory controller (12/510) comprises logic capable of configuring the integrated circuit component (18/670) for operation with a companion integrated circuit component (20/672).

With regard to claim 9, it is clear that memory controller (12/510) comprises logic capable of configuring either the integrated circuit component (18/670) or (20/672) for operation in a stand-alone configuration.

With regard to claim 10, it is clear that the first portion of the system bus is substantially one-half of the system bus and the second portion of the system bus is a remainder of the system bus (see at least column 7, lines 4-9).

With regard to claim 11, Estakhri discloses a system comprising: a plurality of companion integrated circuit components (18/670, 20/672) that collectively implement a logic function embodied in a single, conventional integrated circuit component (shown generally at Fig. 1, 6(a, b), each companion integrated circuit component (one of 18/670, 20/672) comprising: a first logic interface for communicating with a remote component via a portion of a system bus (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "first logic interface" for communicating with a remote component via a portion of a system bus 28/260); a second logic interface for communication with companion logic interfaces of the remaining of the plurality of the integrated circuit components over a separate bus (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "second logic interface" capable of being configured to interface with a companion logic interfaces of the remaining of the plurality of integrated circuit (the other of 18/670 or 20/672) and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus (38/684); and logic (memory controller (12/510) for controlling the selective communication of information received from the first logic interface (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "first logic interface" for

communicating with a remote component via a portion of a system bus 28/260) via the portion of the system bus through the second logic interface to the companion integrated circuit (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "second logic interface" capable of being configured to interface with a companion logic interfaces of the remaining of the plurality of integrated circuit (the other of 18/670 or 20/672) and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus (38/684).

With regard to claim 12, as discussed in claim 11, the logic for controlling the selective communication of information received from the first logic interface through the second logic interface further includes first split bus logic configured to interface with the first logic interface, and second split bus logic configured to interface with the second logic interface (the system bus of Estakhri comprises a first split bus and a second split bus ;see at least column 7, lines 4-9).

With regard to claim 13, the link layer control logic in both first split bus logic and the second split bus logic (it is clear that the controller (12/510) provides unified bus logic configured to consolidate information received from both bus logics), the link layer control logic being configured to exchange link layer control information, such that both the first split bus logic and the second split bus logic possess complete link layer control information for the data being communicated over the system bus (it is clear that the

controller (12/510) provides unified bus logic configured to consolidate information received from both bus logics).

With regard to claims 15-19, see discussion above, since the subject matter presented in claims 15-19 has already been addressed above).

With regard to claim 20, Estakhri discloses an integrated circuit component comprising: a first set of conductive pins for channeling communications with a remote component via a portion of a system bus (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "first logic interface" for communicating with a remote component via a portion of a system bus 28/260; note also that it is inherent that pins must be provided for connections between discrete chips or ICs); a second set of conductive pins for channeling communications with a companion integrated circuit component (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "second logic interface" capable of being configured to interface with a companion logic interfaces of the remaining of the plurality of integrated circuit (the other of 18/670 or 20/672) and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus (38/684); note also that it is inherent that pins must be provided for connections between discrete chips or ICs); additional conductive pins for carrying additional control and communication signals (it is clear that additional pins in addition to the conductive

pins discussed above must be used in the IC of Estakhri); wherein the number of total conductive pins of the integrated circuit component is fewer than the number of conductive pins of a corresponding conventional integrated circuit component (as best the examiner can ascertain, the number of total conductive pins of the integrated circuit component of Estakhri is fewer than the number of conductive pins of a corresponding conventional integrated circuit component, since split bus system is used for each IC component).

With regard to claims 21-23, see discussion above, since the subject matter presented in claims 21-23 has already been addressed above.

With regard to claim 24, it is clear that "conductive pins" must also be provided so that different ICS (as identified above) can be connected to one another.

Response to Arguments

Applicants' arguments filed 8/6/2007 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. As a matter of fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.,* 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification

cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The 112 Rejection (First Paragraph):

Applicants argued that the new limitations added to claim 1, for example) has support from paragraph 0018 of the originally filed specification.

Claim 1 and paragraph 0018 are reproduced below for ease of reference and convenience:

> 1. An integrated circuit component comprising:
> logic capable of being configured to interface with a first portion of a system bus, wherein the first portion of the system bus comprises a first plurality of signal lines of the system bus, but not all of the signal lines of the system bus; and
> logic capable of being configured to interface with a companion integrated circuit and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus, wherein the second portion of the signal bus comprises a second plurality of signal lines of the system bus, which are not a part of the first plurality of signal lines.

> As illustrated in FIG. 1, a conventional configuration includes integrated circuit components 102 and 110 that intercommunicate across a system bus 105. ***In the inventive system 200 of FIG. 2, the system bus 105 is split, so that approximately one half of the bus is directed to integrated circuit component 210, while the remaining portion of the bus 105 is directed to integrated circuit component 211.*** A split bus logic component 214 is provided to interface with the portion of the system bus 105 directed to that particular integrated circuit component. Both integrated circuit components 210 and 211 have blocks denoted by reference numerals 214 and 215. In one embodiment, the circuitry and logic within the split bus logic components 214 and 215 are identical. However, the logic blocks have been denoted with differing reference numerals to indicate a differing functionality, based upon the configuration of those logic blocks. For example, in the configuration illustrated in FIG. 2, the split bus logic blocks 214 are configured to interface with a portion of the system bus 105. Split bus logic blocks 215 are configured to interface with the companion logic block of the companion integrated circuit component. Thus, the split bus logic block 215 of component 210 interfaces directly with the split bus logic block 215 of component 211.

It is clear from claim 1 and paragraph 0018 that "one half of the bus" (paragraph 0018) does not necessarily equal to "the first portion ... comprises a first plurality of signal lines ... but not all the signal lines of the system bus" (claim 1). Similarly, "the remaining portion of the bus" (paragraph 0018) does not necessarily equal to "the second portion ... comprises a second plurality of signal lines ... which are not a part of the first plurality of signal lines" (claim 1).

Thus, it is still the Examiner's position that the new limitations added to claims 1, 11, and 20, in the RCE filed 2/2/2007, do not have adequate support from the originally filed specification. Again, if Applicants disagree, Applicants are required to point to the original filed specification by citing page and line numbers, and to the drawing for support. It is noted that Applicants still have not pointed to the specification by citing page and line numbers, and to the drawings for support of new limitations recited in claim 20.

The 112 Rejection (Second Paragraph):

Applicants argued that "[t]he Office Action rejected claim 20 stating that the language "comprises a plurality of signal of signal lines of the system bus" is unclear. Applicants agree (as this was a clear typo), as have amended claim 20 to delete the duplicative language. The Office Action also stated that the language 'collectively, the conductive pins of the integrated circuit component' is unclear. Applicants suggest that the Examiner consider the entire claim phrase, which reads: 'collectively, the conductive pins of the integrated circuit component do not directly accommodate all signals [sic] lines-of the system bus, but rather directly accommodate fewer than all of the signal lines of the system bus' (emphasis in the original). Applicants submit that this language is clear, and do not understand what the examiner finds unclear about the language. As repeatedly described throughout the specification, the integrated circuit components of embodiments of the invention permit a smaller pin count, by directly connecting to only a portion of the system bus. Accordingly, Applicant submits that claim 20, as amended herein is fully compliant with all statutory requirements, including the requirements of 35 U.S.C. § 112, second paragraph."

At the outset, it is noted that the unclear language (copied from claim 20) cited in the previous Office Action is incomplete (due to a typing error). As a matter of fact, the entire claim phrase was considered. It is still the Examiner's position that it is unclear what may be "the conductive pins" with regard to Figs. 2, 3, and 5; and the "signal lines." Further, it is also unclear what may be the relationships between them. It is

important to note that claim 20 is also rejected under 35 USC 112, 1st paragraph (new matter).

With regard to the rejection of claims 1-24 in view of MPEP 2172.01, Applicants argued that "Applicants hereby note their disagreement with the position taken by the Office Action, and submit that the claims, as filed, recited all necessary or essential interrelationships between the elements. In this regard, Applicants note that each claim element makes appropriate relational reference to other claim elements, such that no element is in isolation and therefore appropriate and proper structural interrelationships among claim elements are properly provided. In addition, the Examiner stated that the claims are indefinite because they allegedly do not recite the required structural interrelationship of "essential elements to the claimed invention." The MPEP, however, does not define what is an 'essential' element, nor did the Examiner provide a definition of what constitutes an 'essential' element."

In response to Applicants' argument, the claimed elements, as defined in the originally filed specification and identified above, are essential elements to the claimed invention. Since they are essential elements as defined by the originally filed specification, their structural cooperative relationships must be provided in the claims. Further, it is clear that the claimed elements as identified above, function simultaneously, are directly functionally related, directly intercooperate, and/or serve independent purposes, as evidenced from the originally filed specification. If Applicants disagree with the Examiner that the above identified elements, as defined by the originally filed specification, are essential elements to the claimed invention, and that

the above identified elements are directly functionally related, directly inter-cooperate, and/or serve independent purposes, it is requested that Applicants provide evidences showing that the identified elements are not essential elements to the claimed invention, do not function simultaneously, are not directly functionally related, do not directly inter-cooperate, and/or do not serve independent purposes; and state on the record that this is the case.

Applicants also argue that "[o]n page 13 of the Office Action, the Examiner states: "the word(s) -connected-- or-operatively connected-- may be used to provide essential structural cooperative relationships between structural elements recited in the claims." As the examiner correctly noted, such term "MAY" be used. However, these terms are not REQUIRED in order for claims to be fully compliant with 35 U.S.C. § 112, second paragraph."

In response to Applicants' argument, Applicants are reminded that in Applicants' previous response, Applicants stated that:

> "Applicants respectfully request the Examiner to provide more helpful insight into this rejection (either by more fully stating the rejection or by providing exemplary language that would overcome the rejection), should the Examiner disagree with Applicants" position and maintain this rejection. In reconsidering this rejection, however, Applicants remind the Examiner that claim breadth should not be confused with indefiniteness (see MPEP 2173.04)."

The Examiner has already offered assistance to Applicants. Specifically, the Examiners has stated that the word "connected" or operatively connected" may be used. Applicants are absolutely correct in stating that "As the examiner correctly noted, such term "MAY" be used." It is appropriate that that the word "MAY" is used by the Examiner because it is entirely up to Applicants whether to incorporate the Examiner's suggestion in order to overcome the rejection.

In addition, Applicants argued that "Applicants respectfully request the Examiner to provide more helpful insight into this rejection, should the Examiner disagree with Applicants' position and maintain this rejection."

As already noted above, Applicants' same request for assistance has already been responded by the Examiner in the previous Office Action. In any event, in response to Applicants' request for assistance, once again, the word(s): -- connected— or –operatively connected – may be used to provide essential structural cooperative relationships between structural elements recited in the claims.

The 102 Rejection:

With regard to claim 1, Applicants argue that "claim 1 is directed to "an integrated circuit component" (i.e., a single component) that includes two separate logic blocks. A first logic block is capable of being configured to interface with a first portion of a system bus. Likewise, the second logic block is capable of being configured to interface with a companion integrated circuit and to receive information that is communicated from the companion integrated circuit, which information was

communicated to the companion integrated circuit via a second portion of the system bus. Simply stated, these features are not disclosed in the '906 patent."

Contrary to Applicants' argument, Estakhri discloses an integrated circuit component (Figs. 1 and 6a) comprising: logic (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises "logic"; see at least column 2, lines 28-37; column 6, lines 57-65) capable of being configured to interface with a first portion of a system bus (28/680; column 1, line 31 to column 2, line 3; column 7, line 1-9); and logic (since 506 is an digital IC and due to the fact that the register must latch to the bus to receive address/data signals, it is clear that the I/O register 22/32 or 671/673 comprises the so-called "logic"; see at least column 2, lines 28-37; column 6, lines 57-65) capable of being configured to interface with a companion integrated circuit (18/670 or 20/672; column 1, line 31 to column 2, line 3; column 6, lines 57-65) and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus (38/684; column 1, line 31 to column 3, line 2; column 7, lines 1-9). Further, it is clear from at least Fig. 6a of Estakhri that the first companion integrated circuit (18/670) and the second companion integrated circuit (20/672) each is disposed in a single integrated circuit chip.

Applicants also argue that "[t]he teachings applied by the Office Action from the '906 patent (disclosing two memory chips 670 and 672 of a memory bank 506) are simply inapplicable to the embodiments defined by claim 1. In this regard, the two

memory chips 670 and 672 of the '906 patent are separate integrated circuits, and not a single integrated circuit as required by claim 1."

Contrary to Applicants' argument, it is clear from at least Fig. 6a of Estakhri that the first companion integrated circuit (18/670) and the second companion integrated circuit (20/672) each is disposed in a single integrated circuit chip.

With regard to **the new matter issue**, Applicants argued that "[s]imply stated, there is no teaching in the '906 patent of a single integrated circuit having logic for interfacing with a first portion of a system bus (the first portion being less than all of the system bus) and second logic for interfacing with a companion integrated circuit to receive information communicated over a second portion of the system bus. As claims 2-10 depend from claim 1, the substantive rejections of those claims should be withdrawn for at least the same reasons."

In response to Applicants' argument, for any language of claim 1 that does not involve "new matter" see the rejection and discussion above. For the "new matter" (see 112, 1st paragraph Rejection above), see column 7, lines 1-9, which is reproduced below for ease of reference and convenience:

> Memory bus 512 includes a flash bus 675 connected to a port 676 of memory I/O unit 652 for transmitting address, data, and command signals between flash memory chips 670, 672 and the memory I/O unit 652. Flash bus 675 includes 16 bit lines, 8 bit lines of which form a first bus 680 connected to a port 682 of I/O register 671 of the first flash memory chip, and another 8 bit lines of which form a second bus 684 connected to a port 686 of I/O register 673 of the second flash memory chip.

With regard to claim 11, Applicants argued that "[l]ike the rejection of claim 1, the Office Action cites memory chips 670 and 672 as comprising the claimed "integrated

circuit." It then cites register 671 as comprising the claimed first logic interface. Then, the Office Action cites the same register 671 as comprising the claimed second logic interface. This rejection simply makes no sense, in the context of the claimed embodiments."

Contrary to Applicants' argument, the word "logic" as claimed simply refers to an **operational** sequence. Different logics can always be programmed into a hardware to provide different operational functions to the hardware. Specifically, Applicants are claiming different logic interfaces, namely "first logic interface" and "second logic interface", provided by an IC component. Applicants are NOT claiming two different and separate structural devices or circuits residing inside an IC component. It is clear that any conventional IC component can provide different logics, not necessarily implemented by hardware, but also by software, to enable the IC component to communication with other ICs or circuitries. In the instant case, it is clear that the I/O register provides logics for the memory chip 670, for example, to enable the memory chip to communicate with the bus or with another memory chip (672, for example). By definition, reading an I/O register involves accessing to its memory. In Estakhri, it is clear that one of the registers 671 and 673 comprises a plurality of logics programmed into the registers.

With regard to claim 20, Applicants argued that "[I]n addition to the rejections copied from claim 1, the Office Action further concluded that "it is inherent that pins must be provided for connections between discrete chips or ICs." Finally, the Office Action alleged that 'the number of total conductive pins of the integrated circuit

component of Estakhri is fewer than the number of conductive pins of a corresponding conventional integrated circuit component, since split bus system is used for each IC component.' In essence, the rejection of claim 20 appears to take the position that the recited features are inherent in the structure recited in claims 1 or 11, and then relies on the rejections of those claims. In response, Applicants repeat and reallege the responsive remarks (above) with respect to the inapplicability of the '906 patent to claims 1 and 11. For the same reasons, the rejection of claim 20 should be withdrawn.

In response to Applicants' argument with respect to "the inapplicability of the '906 patent to claims 1 and 11," Applicants' attention is directed to the rejection and discussion set forth above with respect to claims 1 and 11. Further, it is still the Examiner's position that the number of total conductive pins of the integrated circuit component of Estakhri is fewer than the number of conductive pins of a corresponding conventional integrated circuit component, since split bus system is used for each IC component of Estakhri. As conductive pins must be provided for signal lines of a system bus, a portion of the system bus would require less signal lines and thus, fewer conductive pins. Note that claim 20 is also rejected under 35 USC 112, 1st paragraph.

Duty of Disclosure:

Applicants argued that "Applicants appreciate the Examiner's reminder regarding the duty of disclosure, and Applicant submits that this duty has been fully and properly discharged throughout the prosecution of this application. In response to the Examiner's remarks, however, Applicant wishes to make of record co-pending application serial

number 10/630,260 (which the Examiner indicated that he believed to be a "related" application). That application is presently before the same Examiner (having just received a Decision on Appeal). In addition, the Examiner noted his belief that the present application and the applications of now-issued patents 7,099,994 and 7,103,826 are also inter-related. The undersigned disagrees. The undersigned spoke with Examiner Dang by telephone on July 17, 2007, to better understand Examiner Dang's position on this. In this regard, the present application and the copending '260 application share some common figures and portions of the detailed description are common. Indeed, the undersigned drafted both applications, and explained to the Examiner (in the telephone discussion) that the applications were filed separately because they were believed to be patently distinct inventions. Indeed, the undersigned believes that, had the claims of the two applications been filed in a single application, the Patent Office would have issued a restriction requirement requiring them to be separated. Furthermore, the claims of the two separate cases embody subject matter that is unique to the specifications of each case (and not described in the specification of the co-pending application). For this reason, the two applications have not claimed a formal relationship to each other. The applications of the two now-issued patents noted above have even less relation to the subject matter of the present invention, as both of those patents are directed to RAID memory systems."

In response to Applicants' remark, it is still this Examiner's position that Application No. 10/630,260 and this application (10/630,460) are not only related but also directed to the same subject matter.

With regard to Application No. 10/630,260, the first non-final Office Action was issued on 5/2005; and Applicants subsequently filed an Appeal Brief on 3/2006. A decision from the Board of Appeal has been rendered in favor of the Examiner.

With regard to Application No. 10/630,460, the Examiner was not alerted of the presence of this application until 5/2006. Initially, both Application Nos. 10/630,260 and 10/630,460 were intentionally filed on the same date (7/31/2003).

It is noted that a provisional Obviousness-Type Double Patenting Rejection has not been made in Application No. 10/630,260 because such a rejection would further complicate the issues (112, 102 and 103 Rejections) before the Board of Appeal, and could cause delay in forwarding the application to the Board. Similarly, a provisional Obviousness-Type Double Patenting Rejection and 10/630,240 has not been made while awaiting the Board's decision. Since then, the claims from both applications have been extensively amended. Thus, when one of Application Nos. 10/630,260 and 10/630,240 is issued, all claims from both applications will be considered to determine they are directed to the same subject matter, and thus, an Obviousness-Type Double Patenting Rejection is still appropriate.

Applicants also stated that "the undersigned drafted both applications, and explained to the Examiner (in the telephone discussion) that the applications were filed separately because they were believed to be patently distinct inventions. Indeed, the undersigned believes that, had the claims of the two applications been filed in a single application, the Patent Office would have issued a restriction requirement requiring them to be separated."

Looking back at the two sets of original claims as filed 7/31/2003 from Application Nos. 10/630,260 and 10/630,240, Applicants' above remark does not seem genuine.

For purpose of comparison, the original claim 1 of Application No. 10/630,260 filed 7/31/2003 is reproduced below:

> 1. An integrated circuit component comprising: logic capable of being configured to interface with a first companion integrated circuit and to receive information that is communicated from the first companion integrated circuit, which information was communicated to the first companion integrated circuit via a first portion of a system bus; and logic capable of being configured to interface with a second companion integrated circuit and to receive information that is communicated from the second companion integrated circuit, which information was communicated to the second companion integrated circuit via a second portion of the system bus.

The original claim 1 of Application No. 10/630,460 also filed 7/31/2003 is reproduced below:

> 1. An integrated circuit component comprising: logic capable of being configured to interface with a first portion of a system bus; and logic capable of being configured to interface with a companion integrated circuit and to receive information that is communicated from the companion integrated circuit, which information was communicated to the companion integrated circuit via a second portion of the system bus.

It is clear to the Examiner as well as Applicants that there is absolutely no support for a restriction to be made for the above claims, and therefore no reason for the Examiner to require a restriction requirement. Applicants' statement that the claims are patentably distinct and the "Patent Office would have issued a restriction requirement" for the two claims above is speculative and without any factual support.

Therefore, it is still the Examiner's position that throughout prosecution of this application (10/630,460) and of another pending Application (10/630,260) before this

Examiner, Applicants, in both applications, fail to timely provide this Office with all information known to be material to each application. Specifically, Applicants have filed multiple related applications without providing any information to this Office that these applications are closely related. Applicants are also reminded that "no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct."

With regard to US Patent Nos. 7099994 and 7103826, it is still the Examiner's position that these patents are materially related to Application Nos. 10/630,620 and 10/630,640 are The claims found in US Patent Nos. 7099994 and 7103826 are not entirely directed to "RAID" (Redundant Array of Inexpensive Drives), which by itself, is well-known for its use to provide reliability and performance to the drives. In the instant case, the two integrated circuits shown in Fig. 2 of US Patent Nos. 7099994 and 7103826 are configured in RAID.

Applicants also stated that "[d]uring the telephone discussion, the undersigned inquired of the Examiner whether the Applicant could combine the allowable claims from this application with the allowable claims of the co-pending '460 application, so that only one patent would issue (and therefore require only one set of maintenance fees). Examiner Dang said that such an action may result in a restriction requirement, and that he had not yet considered the claims from that perspective. Instead, the Examiner indicated that he considered the applications be related because they include certain drawing figures, and portions of the specification, in common. Simply stated, the

undersigned disagrees. Notwithstanding, the undersigned does wish to make of record the existence of the co-pending '260 pending application and notes that there is some subject matter overlap between these applications. Therefore, the Examiner should give the co-pending application a level of consideration that the Examiner believes to be appropriate to this application."

In response to Applicants' remark, as noted above, since the filing date of 7/31/2003, the claims from both applications (10/630,260 and 10/630,240) have been extensively amended. The claims in both applications in their current form must be reevaluated as to whether they are directed to the same subject matter. **If Applicants still want to combine the allowable claims of this application and the allowable claims of Application No. 10/630,620, it is suggested that Applicants should let Application No. 10/630,620 go abandoned (express abandonment). At the same time, Applicants should file an RCE for this application, and add the allowable claims of Application No. 10/630,620 to the allowable claims of the RCE of this application. If Applicants need further assistance, Applicants are invited to contact the Examiner to work towards a mutual agreement to further advance prosecution of this application.**

Allowable Subject Matter

Claims 3 and 14 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khanh Dang
Primary Examiner